DOCKET NO. 99-B-186 **PATENT**
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Vidyabhusan Gupta
Serial No.:	09/591,621
Filed:	June 9, 2000
For:	SYSTEM AND METHOD FOR DESIGNING AND OPTIMIZING THE MEMORY OF AN EMBEDDED PROCESSING SYSTEM
Group No.:	2128
Examiner:	Herng-der Day

MAIL STOP AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated in the arguments below, demonstrating the clear legal and factual deficiency of the rejections of some or all claims.

Examiner Day rejected Claims 1-29 under 35 U.S.C. § 102(b) as being anticipated by *Giorgi et al.*, "An Educational Environment for Program Behavior Analysis and Cache Memory Design" ("Giorgi"). This rejection is legally and factually deficient.

The *Giorgi* reference describes an educational software package (Csim) used as a teaching tool in a computer architecture course. (*See Page 1243, left column, 2nd para.*). A user of Csim may build a program and execute the program on an instruction set stimulator to produce a trace file of the memory accesses performed by the program during its simulated execution. (*See Page 1244, left column, 3rd para.*). The trace file then provides input data for analysis tools that allow the user to analyze the performance of the program on one or more specified system architectures. (*See Page 1244, left column, 5th para., through right column, 2nd para.*).

Claim 1 requires a memory access monitor that monitors, during simulated execution of a program, memory accesses by the program to a simulated memory space. This is in distinct contrast to the educational software package of the Giorgi reference, which creates a trace file during simulated program execution, then analyzes the trace file after the simulation has completed.

Examiner Day's response confuses Giorgi's teachings. As Examiner Day notes, Giorgi does indeed teach that "the student traces the execution of the cjpeg program." Giorgi also describes generating the trace file on page 1244, left column, paragraphs 2 and 3, and in Figure 1, as "TRACE".

Claim 1 also requires that "said memory access monitor is capable of generating memory usage statistical data associated with said monitored memory accesses, and wherein said memory accesses comprise read operations and write operations". Giorgi does not teach or suggest that the

trace program is capable of doing this at all. Giorgi teaches that analysis can be performed on the trace file after the execution, but not that memory usage statistical data can be generated by a memory access monitor. In fact, Giorgi describes that these are completely different phases – a trace file is generated during a "program development" phase, and any analysis is done during a "program behavior analysis" phase, a "system behavior analysis" phase, or a "performance analysis" phase. *Figure 1, page 1244, left column paragraph 2 – right column paragraph 1.*

Giorgi does not in any way teach or suggest a memory access monitor as in claim 1, that is both

- capable of monitoring, during said simulated execution of said program, memory accesses to a simulated memory space; and
- capable of generating memory usage statistical data associated with said monitored memory accesses, and wherein said memory accesses comprise read operations and write operations.

Examiner Day responds that the claims to not require that the statistical data be generated at the time of execution. This misses the point that the same memory access monitor must both be capable of monitoring memory access during execution and capable of generating the memory usage statistical data. This feature is not taught or suggested by Giorgi, so Examiner Day's rejection is both legally and factually deficient.

Further, claim 1, and other claims, require a memory optimization controller capable of comparing said memory usage statistical data and one or more design criteria associated with said embedded processing system and, in response to said comparison, determining at least one memory

configuration capable of satisfying said one or more design criteria. At no point does Giorgi's system determine a memory configuration in response to any configuration. At best, Giorgi's system shows that multiple memory configurations can be simulated, then some user can select a memory configuration. As Examiner Day has never shown such a memory optimization controller at all in any art of record. As such, this is a legally deficient anticipation rejection.

For these reasons, Examiner Day's rejection of Claim 1 (and its dependent claims), and independent Claims 8 and 22 (and their dependent claims), are both legally and factually deficient for failing to show plain limitations of the claims in any cited art, and for incorrectly applying the cited art in the anticipation analysis.

As described above, Examiner Day's rejections of all claims are both legally and factually deficient, and it would therefore be inappropriate to put the Applicant to the time and expense of an appeal at this time.

Other distinctions exist, and these matters can be fully discussed on appeal, should that be necessary.

CONCLUSION

As a result of the foregoing, the Applicant asserts that the claims in the Application are in condition for allowance over all art of record, and respectfully requests this case be returned to the Examiner for allowance or, alternatively, further examination.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

MUNCK BUTRUS P.C.

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